VDL TBP ELECTRONICS

"focus on cost drives out quality...

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Design for Test (DfT)

design

| block diagram | schematics | placement | routing | validation |

phase 0
(face to face)

phase 1

phase 2

phase 0

customer delivers tbp
- design idea (in block diagram)
- batch size and year volume of product
- traceability
- component requirements
- test requirements
- quality requirements

tbp delivers customer
- DfT guidelines
- data exchange guidelines
- test access advise (face to face)
- ABC component list

phase 1

customer delivers tbp
- schematics in EDIF 2.0 (or Cadence Allegro format)
- schematics in searchable PDF
- BOM containing MPN, manufacturer and circuit references
- Boundary Scan Description language files
- requirements described in phase 0

tbp delivers customer
DfT report* containing:
- preliminary testcoverage
- preliminary teststrategy
- preliminary slip through
- test access recommendations
- board complexity index

phase 2

customer delivers tbp
- ODB ++ (CAD data)
- schematics in searchable pdf
- BOM containing MPN, manufacturer and circuit references
- requirements described in phase 0

tbp delivers customer
final DfT report* containing:
- final testcoverage
- final teststrategy
- percentage slip through
- test access recommendations
- board complexity index

* if planned in advance, VDL TBP Electronics will deliver DfX reports - regarding only one design - within 72 hours delivery time